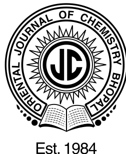

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Enhanced Characteristics of Square-Shaped Extended Source TFET Via Silicon Carbide Polytype (3C-SiC) and a Dopant Pocket Layer

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ABSTRACT

In this paper, for the first time, the square-shaped extended source tunneling field-effect transistor (SES TFET) by means of the silicon carbide polytype (3C-SiC) and dopant pocket layer has been presented. By inserting the silicon carbide polytype as substrate and n-type pocket in the channel at the source edge, on-current is increased by about 10 times compared with the conventional SES TFET because of the reduced losses and energy band modification imposed by the silicon carbide and pocket doping, respectively. Additionally, using calibrated simulations, the SES TFET with 3C-SiC substrate and dopant pocket layer is evaluated in terms of various radio-frequency (RF) parameters, including the gate to source capacitance, gate to drain capacitance, trans conductance, channel resistance, transport time delay, cutoff and maximum oscillation frequencies. The simulation results of the SES TFET with the 3C-SiC substrate and dopant pocket layer exhibits a superior switching-state current ratio (~10^{13}) and a small transport time delay (about 0.15 psec) that is a hopeful candidate for conventional SES TFET.

Keywords: Silicon carbide polytype (3C-SiC); Cubic zinc-blende; Transport time delay; Switching-state current ratio; Dopant pocket layer; Tunneling field-effect transistors (TFETs).

INTRODUCTION

Over the past few years, silicon carbide (SiC) poly types have been concerned as the alternative semiconductor materials for future high temperature power semiconductor devices at high frequency with reduced power losses and die size because of their large breakdown and drift velocity in saturation state; sensibly high mobility, and reasonably good thermal conductivity[1-5]. The first commercial silicon carbide devices were obtained as high power Schottky diodes in year 2001[6].

There are many different polytypes of SiC (over 200), including cubic, hexagonal and rhombohedral variants, where they have widely

ranging physical properties. They are variations of the same chemical compound that are identical in two dimensions and differ in the third (different stacking sequences). Therefore, each of them exhibit different electrical, optical and thermal properties. The Si-C bilayers atomic stacking sequences along [111] direction determine all the its polytypes, the most common amongst which are zinc-blende structure that Si and C inhabit ordered positions in a diamond structure; hexagonal (2H, 4H and 6H) or α-SiC and rhombohedral (15R) type SiC that stated to as $\alpha\eta$-SiC, n Si-C bilayers include stack of C and Si layers in the primitive cell[2,5]. Due to the reduced scattering resulting from the breaking of an out-of-plane symmetry selection rule, 3C-SiC has the highest electron mobility and saturation velocity[5]. Figures 1 and 2 show the lattice structures and distribution in circumstellar 3C-SiC by means of transmission-electron-microscopy (TEM) on presolar silicon carbide in the Murchison carbonaceous chondrite[7], which is most important for this paper.

One of the promising new developments in the semiconductor transistors research is tunneling field-effect transistor (TFET) due to the its low subthreshold swing and low off-state leakage current[8,15]. Its current is based on the tunneling effect at the source to channel edge. Therefore, TFETs can overcome the supply voltage scaling issues, the 60 mV/decade subthreshold slope and power consumption limits of MOSFET devices at room temperature[16,17]. Due to the insignificant band-to-band tunneling phenomenon in silicon TFETs, they have low on-currents that one of the major concerns in the design and fabrication of these transistors is to improve their on-current performance. On the other hand, an increase in on-current causes the RF performances of the TFETs to be enhanced. To enhance the TFET on-currents, many efforts have been made including hetero-structures[11,16,17], band-gap engineering[18,20], high mobility and low band-gap materials[20,23], high-k dielectric materials[24,25], hetero-gate-dielectric (HG)[26,27], dual material gate[28,30] and vertical direction tunneling[31,32].

In order to enhance the on-state current and the other device performance parameter, another

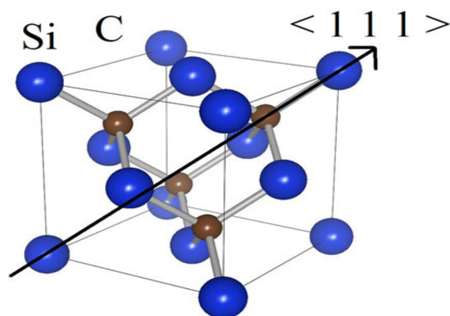
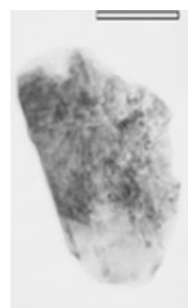
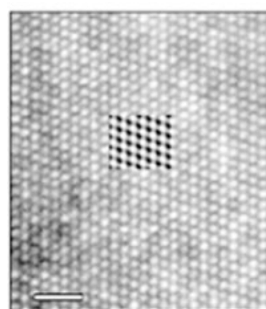


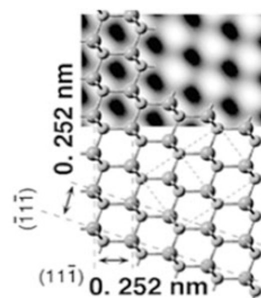
Fig. 1: The crystal structure of cubic silicon carbide polytype (3C-SiC).



(a)



(b)



(c)

Fig. 2: The polytype distribution in circumstellar 3C-SiC from the Murchison carbonaceous chondrite[10]. (a) TEM image with scale bar of 0.1 µm, (b) high-resolution transmission-electron-microscopy (HRTEM) image with scale bar of 1 nm, and (c) atomic model of the 3C-SiC zone axis superimposed on a simulated lattice image.

method of revising the basic TFET architecture has been reported by adding a pocket doping region between the source and channel[33]. This pocket causes a stronger magnitude of electric field and consequently a shorter tunneling distance and results in improved DC and RF performances as well as a better reliability compared to the conventional TFETs[25,32,34].

On the other hand, we recently presented the DC and RF performances of double-gate SES TFETs[35,37]. In this paper, in order to further enhance the device performance, the 3C-SiC substrate and an n-type pocket in the channel at the source edge of SES TFET have been placed and its performance is compared with conventional SES TFET with similar dimensions. The simulation results show that the SES TFET with 3C-SiC substrate and dopant pocket layer exhibits higher on-current, higher switching-state current ratio and smaller transport time delay than those of the conventional SES TFET.

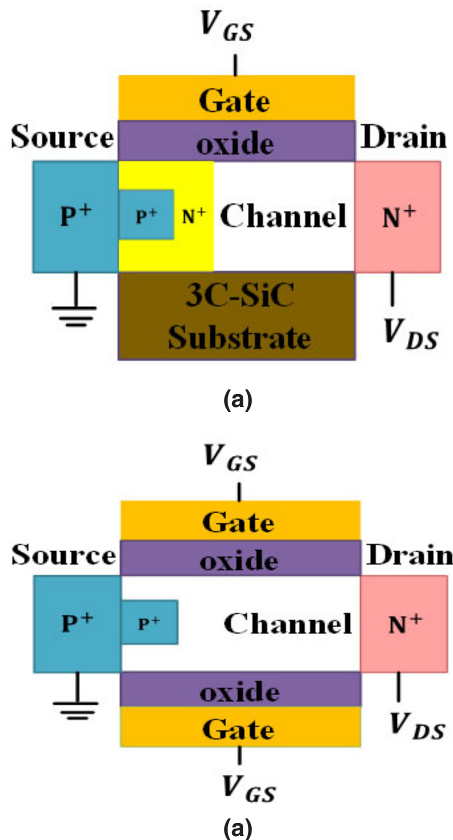


Fig. 3: Schematic structure of (a) the SES TFET with 3C-SiC substrate and dopant pocket and (b) the conventional SES TFET[38].

This paper is structured and organized as follows. The structure, model and its validation are described in section 2. Section 3 presents the results and discussion while the final Section shows concluding remarks.

Structure, Model and its validation

The cross-sectional views of the SES TFET with 3C-SiC substrate and dopant pocket layer and the conventional SES TFET are shown in Figure 3. Recently, the DG silicon-based TFET structure has been demonstrated experimentally[38]. On the one hand, the heavily doped pocket region can be achieved by a tilt angled implant before the gate stack formation[31]. On the other hand, we recently presented the process flow by high-energy and low-current boron implantation with another mask after the pocket formation to fabricate the SES TFET[35].

Two simulated structures have gate length of 30 nm, body thickness of 15 nm and gate oxide thickness of 2 nm. The channel, source and drain doping concentrations of the structures were 10^{15}, 10^{20} and 10^{20} cm^{-3}, respectively. For the SES TFET with the dopant pocket, a heavily doped pocket with doping concentration of 10^{19} cm^{-3} at the source channel interface is structured.

All the device simulations were done in Silvaco ATLAS software[39]. For superior accuracy, the BTBT model was included using a non-local path tunneling model in the simulations. Furthermore, the Shockley–Read–Hall and Auger recombinations; concentration dependent mobility,

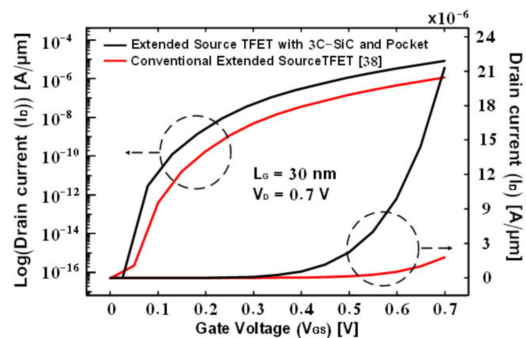


Fig. 4: Variation of drain current in linear and logarithm scales versus VGS for the SES TFET with 3C-SiC substrate and pocket and the conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V.

bandgap narrowing effect, field dependent mobility and trap–assisted tunneling (TAT) models were used to model the recombination and generation in the highly doped regions. Also, we recently presented the validation of our simulation non-local BTBT model by tuning of the effective electron and hole masses as done in our earlier works[13,15,23,35,40].

RESULTS AND DISCUSSION

The effect of the 3C-SiC substrate and dopant pocket on the drain current of a SES TFET with 30 nm gate length versus the gate voltage (V_{GS}) in linear and logarithm scales biased at the constant drain voltage (V_D = 0.7 V) is shown in Figure 4. As seen, the extended source TFET with the 3C-SiC substrate and pocket exhibits higher on-current (more than 10 times) as compared to conventional extended source TFET due to the increase in the BTBT generation rate and reduced losses. This improvement in the BTBT generation rate is due to the existence of the n-type pocket at source and the channel interface. In the other words, the barrier width at the interface of source and channel is decreased for a TFET with the dopant pocket layer, which helps in the total electric field and drive current improvement, as mentioned in the Refs.[25, 31,34].

Figure 5 illustrates the alteration of trans conductance (g_m) versus V_{GS} for the extended source TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length. It is

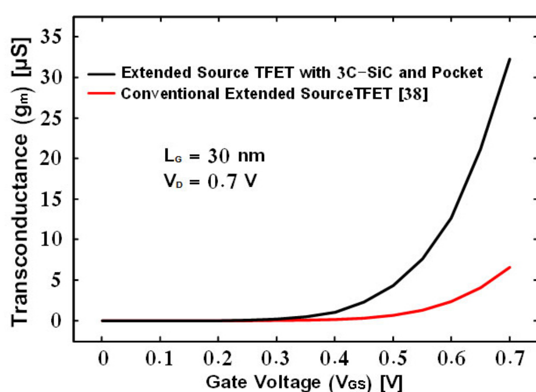


Fig. 5: Variation of transconductance (gm) versus of V_{GS} for the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V.

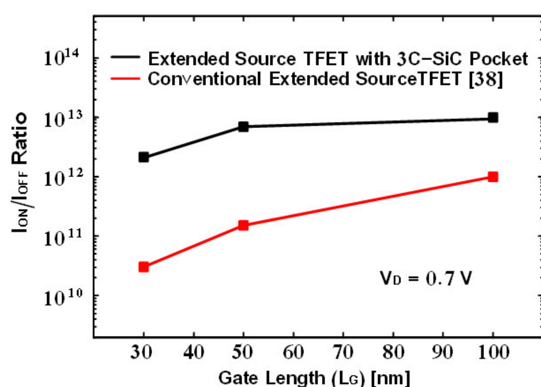


Fig. 6: Comparison of the switching state current ratio value between the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET at drain voltage of 0.7 V.

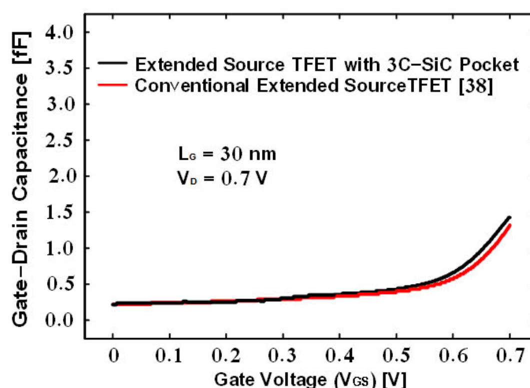


Fig. 7: The gate voltage dependence of gate to drain capacitance of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V.

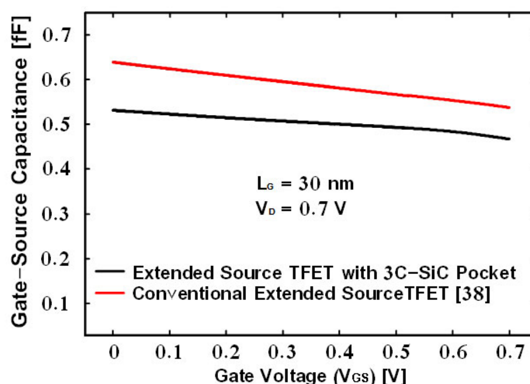


Fig. 8: The gate voltage dependence of gate to source capacitance of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V.

evident that the extended source TFET with 3C-SiC substrate and pocket has higher trans conductance values than the conventional extended source TFET because the improvement of drain current leads to an increase in the trans conductance.

Figure 6 compares the switching-state current ratio for the extended source TFET with 3C-SiC substrate and pocket and conventional extended source TFET at drain voltage of 0.7 V. The current at off and on states are defined as the minimum value of drain current (as the current when V_{GS}=0 V and V_{DS}= 0.7 V) and the value of current when V_{GS} = V_{DS} = 0.7 V, respectively. As can be seen, the switching-state current ratio improves for he extended source TFET with 3C-SiC substrate and pocket. Its value is about 10^{13} for 100 nm extended source TFET with pocket.

Figures 7 and 8 show the gate voltage dependent gate to drain and gate to source capacitances of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V, respectively. The lower gate to source capacitance in the extended source TFET with 3C-SiC substrate and pocket is due to the barrier width reduction at the source to channel edge. However, due to the inversion layer extension from the drain-side toward the source-side, the dominant capacitance between the gate and the inversion layer under a TFET gate is gate-drain capacitance[25,35].

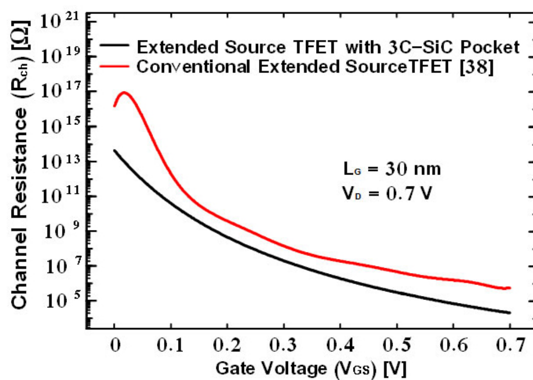


Fig. 9: Channel resistance of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length biased at drain voltage of 0.7 V versus V_{GS}.

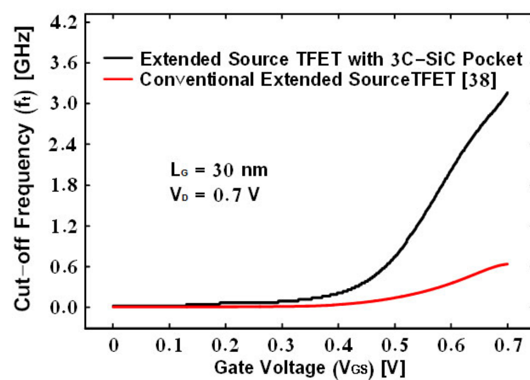


Fig. 11: Cutoff frequency of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with variation of V_{GS} at drain voltage of 0.7 V.

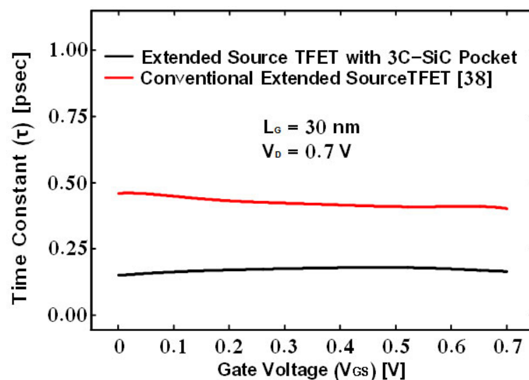


Fig. 10: Transport time delay of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length biased at drain voltage of 0.7 V versus of V_{GS}.

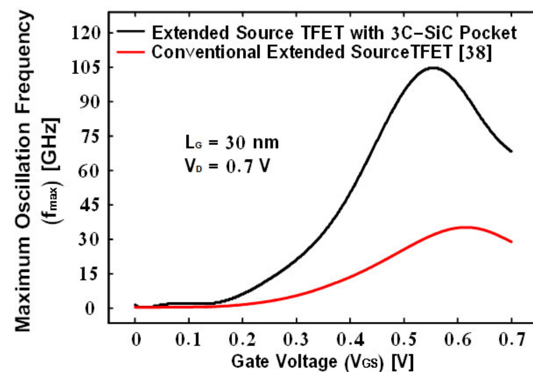


Fig. 12: Maximum oscillation frequency of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with variation of V_{GS} at drain voltage of 0.7 V.

Figure 9 illustrates the effect of the 3C-SiC substrate and dopant pocket on the channel resistance (R_{ch}) of a SES TFET with 30 nm gate length versus the gate voltage biased at drain voltage of 0.7 V. It can be seen that the channel resistance value of the SES TFET with 3C-SiC substrate and pocket is much lower than that of the conventional SES TFET due to the high channel conductivity induced the existence of the n-type pocket at the interface of source and channel.

The channel resistance of the device plays a crucial role in determining transport time delay since $R_{ch} \times C_{gd}$ acts as an index for showing of the channel charges response speed to gate signal[25,35]. The variation in the transport time delay versus the gate voltage for the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length at drain voltage of 0.7 V is shown in Figure 10. As can be confirmed from Figure 9, due to the smaller resistance of channel, the transport time delay for the SES TFET with 3C-SiC substrate and pocket (about 0.15 psec) is much lower than that of conventional SES TFET.

The cutoff and maximum oscillation frequencies are considered as figures of merit (FoM) for frequency response in the high frequency application. The RF performances of the SES TFET with 3C-SiC substrate and pocket are considered by extracting the cutoff and maximum oscillation frequencies and are compared with the conventional SES TFET. The cutoff and maximum oscillation frequencies are frequencies at which the current and unilateral power gains of a TFET drops to unity, respectively[25,35]. Figure 11 displays the gate capacitance values of cutoff frequency for the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length as versus the gate voltage biased at drain voltage of 0.7 V. It is observed that the extended source TFET with 3C-SiC substrate and pocket shows better value of cutoff frequency when compared with that of the conventional SES TFET due to its higher transconductance, as shown in Figure 5.

Figure 12 shows the variation of maximum oscillation frequency of the SES TFET with 3C-SiC substrate and pocket and conventional SES TFET with 30 nm gate length versus the gate voltage at drain voltage of 0.7 V. It is evident that the extended source TFET with 3C-SiC substrate and pocket has higher maximum oscillation frequency than that of the conventional extended source TFET because it shows lower channel resistance and higher cutoff frequency, as seen in in Figures 9 and 11.

CONCLUSIONS

In this paper, we report a detailed study of the SES TFET with 3C-SiC substrate and dopant pocket layer. The variation in the DC and RF performances including the drain current, switching-state current ratio, gate to source capacitance, gate to drain capacitance, transconductance, channel resistance, transport time delay, cutoff frequency and maximum oscillation frequency as a function of gate voltage has been analyzed. The presence of the silicon carbide polytype as substrate and pocket in the channel at the source edge provides higher on-current about 10 times when compared with the conventional extended source TFET. A higher switching-state current ratio (~10^{13}), a smaller transport time delay (about 0.15 psec); and excellent cutoff and maximum oscillation frequencies were obtained, indicating that the SES TFET with 3C-SiC substrate and dopant pocket is a good candidate as a replacement for the conventional TFETs in future low power applications.

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